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10EE764

Seventh Semester B.E. Degree Examination, Dec.2018/Jan. 2019
VLSI Circuits and Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With neat diagrams, explain the working of enticement mode nMOS transistor, for different values of V_{DS}. **(08 Marks)**

b. Explain the nMOS fabrication process with neat diagram. **(10 Marks)**

c. Compare CMOS and bipolar techniques. **(02 Marks)**

2 a. Discuss the drain to source I_{ds} versus V_{ds} relationship for non saturated and saturated regions. **(10 Marks)**

b. Define Z_{pu} Z_{dp}. Show that pull-up to pull-down ratio for nMOS inverter driven through one or more pass transistor is $\frac{Z_{pu_2}}{Z_{pd_2}} = 8:1$. **(10 Marks)**

3 a. With neat diagrams express the Lambda based design rules as applicable to MOS layers, transistors, and contracts. **(10 Marks)**

b. Draw circuit symbol and stick diagram for CMOS inverter. **(04 Marks)**

c. Draw the stick diagram and layout for an nMOS two way selector, with enable input. **(06 Marks)**

4 a. What is sheet resistance? Calculate sheet resistance of transistor channel if L = 8λ, W = 2λ, if n transistor channel $R_s = 10^4\Omega$/square. **(06 Marks)**

b. Derive an expression for rise time and fall time of CMOS inverter. **(06 Marks)**

c. Write a note on BiCMOS drivers. **(08 Marks)**

PART – B

5 a. Explain different scaling models by considering the relevant diagram of an nMOS transistor. **(06 Marks)**

b. Obtain the scaling factors for the following transistor parameters, by considering the constant voltage scalling model :
   i) Gate area
   ii) Gate capacitance per unit area
   iii) Gate capacitance. **(06 Marks)**

c. By considering a suitable example, compare the metal inter connect and elector-optical interconnect models. **(08 Marks)**

6 a. Explain the structured design approach for a parity generator circuit and draw the nMOS diagram of the basic cell. **(10 Marks)**

b. Explain the structured design of bus arbitration logic for n lines. Also write the circuit diagram and stick diagram for a single cell. **(10 Marks)**

7 a. Explain the basic bus architecture for 4 bit arithmetic process with neat diagrams. **(10 Marks)**

b. Explain with neat diagram 4 × 4 barrel shifter. **(10 Marks)**

8 a. Define explain regularity. **(04 Marks)**

b. Explain the design of 4-bit adder with adder element requirements. **(08 Marks)**

c. Draw the structure of a multiplexer based adder logic with stored and buffered sum output. **(08 Marks)**

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